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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/787,029 | 02/25/2004 | Daniel Boyko | A0312.70513US00 | 3915 |

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| EXAMINER | |
|---|---|
| COX, CASSANDRA F | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 02/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/787,029 | BOYKO ET AL. | |
| | Examiner | Art Unit | |
| | Cassandra Cox | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *3-9 and 11-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-15,19-27 and 30* is/are allowed.

6)☒ Claim(s) *3,4,8,9,11 and 18* is/are rejected.

7)☒ Claim(s) *5-7,16,17,28 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 3-4, 8-9, 11, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Sumi (U.S. Patent No. 6,522,183).

In reference to claim 9, Sumi discloses in Figure 1 a device having a clock generation circuit (105) comprising: a) a phase locked loop (109, 125, 126, 112, 116) having an output (F01); b) a first programmable frequency scaling circuit (113) having an input and an output, the input being coupled to the output (F01) of the phase locked loop, and the output of the first programmable frequency scaling circuit (113) providing a first clock signal (FV11); c) a second programmable frequency scaling circuit (114) having an input and an output, the input being coupled to the output (F01) of the phase locked loop, and the output of the second programmable frequency scaling circuit (114) supplying a second clock signal (FV12); and d) at least one control register (117), having a field (117a) specifying a scale factor of the first frequency scaling circuit (113) and a field (117b) specifying a scale factor of the second frequency scaling circuit (114).

In reference to claim 3, Sumi discloses in Figure 1 that the first and second programmable frequency scaling circuits are programmable dividers.

In reference to claim 4, Sumi discloses in the ABSTRACT that the first and second programmable dividers may alternatively be counters.

In reference to claim 8, Sumi discloses in Figure 1that the phase locked loop (109, 125, 112, 116) additionally comprises a third programmable divider (116).

In reference to claim 11, Sumi discloses in Figure 1 circuit having an associated method of operating comprising: a) providing a reference clock (FR11); b) specifying a first frequency ratio between a first clock (FV11) and the reference clock (FR11); c) deriving the first clock from the reference clock with the first frequency ratio (this is achieved by programming divider 113); d) specifying a second frequency ratio between a second clock (FV12) and the reference clock (FR11); e) deriving the second clock from the reference clock with the second frequency ratio (this is achieved by programming divider 114); f) clock first circuitry with the first clock (FV11) and clocking second circuitry with the second clock (FV12); and g) changing the frequency of the first clock on the fly (see column 7, lines 37-44, wherein the frequency can be changed by a user changing a station selection key 131).

In reference to claim 18, Sumi also discloses in Figure 1 wherein the device comprises at least one control register (117) with a field (117a) specifying a frequency ratio between the reference clock (FR11) and the first clock (FV11) and a field (117b) specifying a frequency ratio between the reference clock (FR11) and the second clock (FV12).

***Allowable Subject Matter***

4. Claims 12-15, 19-27, and 30 are allowed.

5. Claims 5-7, 16-17, and 28-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: Claims 5-7 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the device additionally comprises control logic (350) in combination with the rest of the limitations of the base claims and any intervening claims. Claim 16 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the method includes placing the chip in a first power saving mode by changing the first frequency ratio such that the first circuitry is clocked at a lower rate without changing the frequency of the reference clock or the second clock in combination with the rest of the limitations of the base claims and any intervening claims. Claim 17 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 4A wherein the frequency of the first clock (CCLK) and the frequency of the second clock (SCLK) are not integer multiples of each other in combination with the rest of the limitations of the base claims and any intervening claims. Claims 28-29 would be allowable because the closest prior art of record fails to disclose a circuit including at least one interface circuit clocked by the second clock signal (SCLK) and adapted to interface to external circuitry in combination with the rest of the limitations of the base claims and any intervening claims.

7. The following is an examiner's statement of reasons for allowance: Claims 12-15, 26-27, and 30 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 3 wherein the method includes placing the chip in a first power saving mode by changing the first frequency ratio such that the first circuitry is clocked at a lower rate in combination with the rest of the limitations of the base claims and any intervening claims. Claims 19-25 are allowed because the closest prior art of record fails to disclose a circuit wherein the method includes waiting until a defined time relative to the period of the second clock (SCLK) while holding the state of the first clock; and loading the new value in a control location at the defined time in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

CC

February 17, 2006

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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